

Realization of Four-Terminal Switching Lattices: Technology Development and Circuit Modeling

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Abstract—Our European Union’s Horizon-2020 project aims to develop a complete synthesis and performance optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer. Within the project, we investigate different computing models based on either two-terminal switches, realized with field effect transistors, resistive and diode devices, or four-terminal switches. Although a four-terminal switch based model offers a significant area advantage, its realization at the technology level needs further justifications and raises a number of questions about its feasibility. In this study, we answer these questions. First, by using three dimensional technology computer-aided design (TCAD) simulations, we show that four-terminal switches can be directly implemented with the CMOS technology. For this purpose, we try different semiconductor gate materials in different formations of geometric shapes. Then, by fitting the TCAD simulation data to the standard CMOS current-voltage equations, we develop a Spice model of a four-terminal switch. Finally, we successfully perform Spice circuit simulations on four-terminal switches with different sizes. As a follow-up work within the project, we will proceed to the fabrication step.

Index Terms—emerging technologies, four-terminal switching lattice, technology simulation, device modeling, circuit analysis

I. INTRODUCTION

Our European Union’s Horizon-2020 project, named acronym of NANOxCOMP, aims to develop a complete synthesis and optimization methodology for nano-crossbar arrays. It contributes to the construction of emerging computers by proposing nano-crossbar based computer architectures. In the first half of our four-year project, we have investigated different computing models suitable for the crossbar arrays by considering their effect on circuit performance in terms mostly of area, *i.e.*, array size [1]–[4].

Computing with crossbar arrays is achieved by its cross-points behaving as switches, either two-terminal or four-terminal, as shown in Fig.1. Depending on the technology used, a two-terminal switch behaves as a diode [5], [6], a resistive/memristive switch [7], or a field effect transistor (FET) [8]. Diode and resistive switches correspond to the

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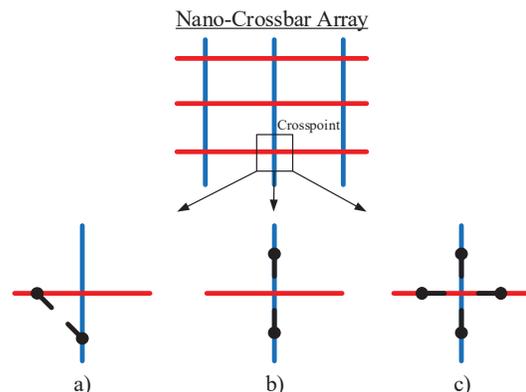


Fig. 1. Switching models of a nano-crossbar array: crosspoint as a) two-terminal switch with terminals in the crossed lines; b) two-terminal switch with terminals in the same line; c) four-terminal switch.

crosspoint structure in Fig. 1a), where the switch is controlled by the voltage difference between the terminals. Fig. 1b) shows a FET based switch, where the horizontal red line represents the controlling input. A four-terminal switch is given in Fig. 1c). The controlling input, not shown in this figure, has a separate physical formation from the crossbar [9].

Comparing the number of switches required to implement a given logic function, we see that the four-terminal switch based arrays are superior than the two-terminal based ones [1]. In these comparisons, the resistive/memristive arrays are not taken into account. However, it is not hard to guess that their sizes are much worse than those of the diode and FET based arrays. The reason is that the resistive arrays use a minterm/maxterm representation of a given logic function such that each minterm/maxterm is implemented by a crossbar line [10], [11]. The diode and FET based arrays do not have such restrictions and thus, the minimal sum of product forms can be used for each product implemented by a line [8], [12]. As a result, the four-terminal switch based arrays have an important advantage in area. Indeed, this is not surprising, since they use two dimensional paths to implement the products of a given function as opposed to the two-terminal switch based arrays using one dimensional paths (crossbar lines).

Within the second half of our project, we further investigate the four-terminal switch based arrays, called switching

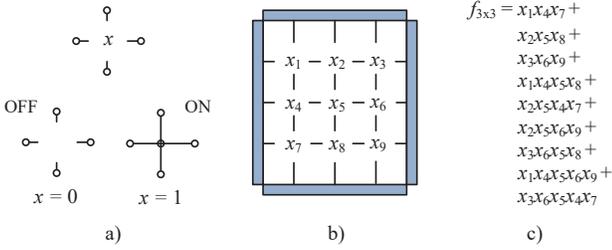


Fig. 2. Illustration of a) four-terminal switch; b) 3×3 four-terminal switching network; c) 3×3 switching lattice function.

lattices, now in technology level. The literature lacks concrete justifications for device realization of switching lattices. In this study, we aim to explore different ways of implementing a switching lattice. To do so, first, we develop a technology for a four-terminal switch, based on the CMOS technology with similar current-voltage (I-V) characteristics. For this purpose, we investigate different semiconductor gate materials and geometric shapes with the support of the three dimensional (3D) technology computer-aided design (TCAD) simulations. Second, we construct a model for the four-terminal switch consisting of six CMOS transistors. The parameters of the CMOS I-V equations are extracted from the TCAD simulation data and a Spice model is developed. Finally, we successfully perform Spice circuit simulations on switching lattices with different sizes. Experimental results validate the computational circuits as well as provide options for new materials and designs suitable for the design of four-terminal switches. Our next plan is to complete a clean room experimental validation.

The rest of this paper is organized as follows. Section II presents the switching lattices and describes how Boolean functions can be realized using switching lattices. Section III explains how we develop a technology for a four-terminal switch in support of TCAD simulations. Section IV introduces the circuit modeling of a four-terminal switch. Section V describes the circuit implementations of switching lattices using Spice simulations. Section VI concludes the paper including the learned lessons and future plans.

II. LOGIC SYNTHESIS USING SWITCHING LATTICES

A four-terminal switch is shown in Fig. 2a). All its terminals are either disconnected (OFF) if its control input x has the value 0, or connected (ON), otherwise. A switching lattice is formed as a network of four-terminal switches, where each switch is connected to its horizontal and vertical neighbors. For example, the 3×3 switching network, where $x_1 \dots x_9$ denote the control inputs of switches, is shown in Fig. 2b). The lattice function, whose inputs are the control inputs of switches, evaluates to 1 if there is a path between the top and bottom plates of the lattice and is written as the sum of products of control inputs of switches in each path. The function of the 3×3 lattice, *i.e.*, $f_{3 \times 3}$, is given in Fig. 2c). Note that a lattice function is unique and does not include any redundant products, *e.g.*, a possible path $x_3x_2x_1x_4x_7$ in the 3×3 switching network is eliminated by the path $x_1x_4x_7$ [3].

Table I presents the number of products in an $m \times n$ lattice function, where $2 \leq m, n \leq 9$. Observe that as the lattice

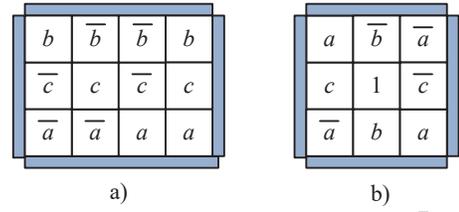


Fig. 3. Realizations of the function of XOR₃ gate, $out = \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc$, using switching lattices: a) 3×4 ; b) 3×3 .

TABLE I
NUMBER OF PRODUCTS IN AN $m \times n$ LATTICE FUNCTION.

m/n	2	3	4	5	6	7	8	9
2	2	3	4	5	6	7	8	9
3	4	9	16	25	36	49	64	81
4	6	17	36	67	118	203	344	575
5	10	37	94	205	436	957	2146	4773
6	16	77	236	621	1668	4883	14880	44331
7	26	163	602	1905	6562	26317	110838	446595
8	42	343	1528	5835	25686	139231	797048	4288707
9	68	723	3882	17873	100294	723153	5509834	38930447

size increases, the number of products in the lattice functions increases dramatically, indicating the lattices that can be used to realize a rich variety of logic functions [3]. Moreover, for the lattices with sizes very close to each other, there exist a wide range of functions with different number of products. For example, while $f_{6 \times 8}$ contains 14880 products, $f_{7 \times 7}$ has 26317 products. This is also true for the lattices with the same size. For example, while $f_{6 \times 6}$ includes 1668 products, $f_{9 \times 4}$ has 3882 products. It can be observed from Table I that there exist a number of possible lattices to realize a given logic function, enabling the designer to choose the most appropriate one that fits best in the design.

In recent years, efficient algorithms have been introduced for the synthesis of logic functions using switching lattices [2]–[4], [13]. These algorithms realize a logic function by simply mapping the appropriate literals of the logic function and/or constant values (0 and 1) to the control inputs of switches. While doing so, they aim to use a minimum number of switches, *i.e.*, a lattice with minimum size. As an example, Fig. 3 depicts the realizations of a 3-bit XOR gate, XOR₃, using the 3×4 lattice and the one with the minimum size, *i.e.*, 3×3 .

III. REALIZATION OF SWITCHING LATTICES

In this section, we introduce the developed technology for the four-terminal switch with TCAD simulation results.

A. Technology Development

While developing the technology, we consider two main criteria: 1) considering the symmetry among four terminals, the I-V relationship of terminal pairs should be similar to each other; 2) a single gate to control all current paths between terminal pairs. Since there are 6 possible pair of terminals, computed as $C(4, 2)$, where C stands for the combinations, we have 6 different current paths or channels. Note that in a conventional CMOS transistor, there is a single current path between its source and drain terminals.

We consider three different types for the realization of a four-terminal device, *i.e.*, square shaped gate, cross shaped gate, and junctionless, as shown in Fig. 4. A square shaped substrate is used for the sake of symmetry in all devices. Note

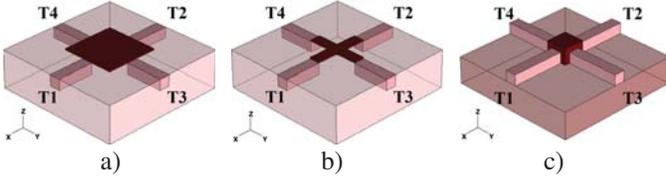


Fig. 4. Shape of devices and electrode structures: a) square; b) cross; c) junctionless.

TABLE II
STRUCTURAL FEATURES OF FOUR-TERMINAL DEVICES FOR TCAD SIMULATIONS.

Device type	Enhancement		Depletion (Junctionless)
	Square Shaped	Cross Shaped	
Device size (nm)	2400 × 2400 × 730	2400 × 2400 × 730	24 × 24 × 8
Electrode size (nm)	700 × 200 × 200	700 × 200 × 200	24 × 2 × 2
Gate size (nm)	1000 × 1000 × 30	W:200, H:30	4 × 4 × 3
Doping profile (cm ⁻³)	Substrate: B, 10 ¹⁷ Electrodes: P, 10 ²⁰	Substrate: B, 10 ¹⁷ Electrodes: P, 10 ²⁰	Electrodes: P, 10 ²⁰
Gate material	SiO ₂ , HfO ₂	SiO ₂ , HfO ₂	SiO ₂ , HfO ₂
Electrode material	n-type Si	n-type Si	n-type Si
Substrate material	p-type Si	p-type Si	SiO ₂

that the square and cross shaped devices are enhancement type and the junctionless device is a depletion type. The channel width and length ($W : L$) ratios for the mentioned 6 different paths should also be very close to each other. Additionally, short-channel effects should be avoided.

Thus, for the enhancement type devices, we select the same dimensions for all four electrodes so that the W values become the same. The distances between electrodes, denoted as L_s , are selected close to each other. The L values are selected larger than the W values to eliminate the short-channel effects. It was observed that the use of a cross shaped device allows us to have almost the same W values, and thus, its device symmetry is better than that of the squared shaped device. For the depletion type devices, we use a gate formation similar to those used in all-around gate transistors. Thus, high level of gate control is achieved.

Also, conventional silicon dioxide (SiO₂) and high dielectric hafnium dioxide (HfO₂) gate materials are used to observe the effect of dielectric constant. Si-based enhancement type devices are simulated with 10¹⁷cm⁻³ boron (B) doped p-type substrate, 10²⁰cm⁻³ phosphorus (P) doped n-type electrodes, and high-k dielectric oxide gate to form the pn-junctions under electrical field. A similar methodology is used for the depletion type junctionless device with n-type Si electrodes only. The features of four-terminal devices are summarized in Table II.

B. TCAD Simulation

We use three different simulation set-ups: 1) obtaining the drain-source current (I_{DS})-gate source voltage (V_{GS}) curves when the drain-source voltage (V_{DS}) is 10mV; 2) obtaining I_{DS} - V_{GS} curves when V_{DS} is 5V; 3) obtaining I_{DS} - V_{DS} curves when V_{GS} is 5V. For these set-ups, the source voltage is always set to 0V.

The configuration of a typical run is based on the applied voltage and current vectors over the four-terminal electrodes. If the current is towards device, it is referred as drain (D) otherwise, it is called as source (S). We note that the four

terminal electrodes have fixed locations and are named as T1, T2, T3, and T4. We explored 16 different cases in the symmetric and non-symmetric operating conditions, where the terminals are used as drain or source electrodes or float (F), where a terminal is connected to nothing. These cases can be given as 1 drain-1 source (DSFF, SFDF), 1 drain-3 sources (DSSS, SDSS, SSDS, SSSD), 2 drain-2 sources (DDSS, SDDS, DSDD, DSSD, SDSD, SSDD) and 3 drains-1 source (DDDS, SDDD, DDDSD, DSDD). As an example, the DSSS case means that T1 is drain, the other terminals are source.

Fig. 5 presents the TCAD simulation results on the threshold voltage runs and saturation profile I-V for the DSSS case on the enhancement type square shaped device with the HfO₂ gate material. Moreover, Fig. 8a) presents the current density vector profile on the square shaped device which shows the effect of electrical field on the junction characteristics.

It is observed that while the device with the HfO₂ gate material has a threshold voltage V_{th} value close to 0.16V and an on/off ratio (I_{on}/I_{off}) equal to 10⁶, the device with the SiO₂ gate material has a V_{th} value close to 1.36V and an on/off ratio equal to 10⁵. Note that I_{on} and I_{off} denote the drain current when V_{GS} is 5V and 0V, respectively, while V_{DS} is 5V.

Fig. 6 presents the TCAD simulation results for the enhancement type cross shaped device with the HfO₂ gate material under the DSSS case. Also, its current density vector profile is given in Fig. 8b).

It is observed that while the device with the HfO₂ gate material has a V_{th} value close to 0.27V and an on/off ratio equal to 10⁶, the device with the SiO₂ gate material has a V_{th} value close to 1.76V and an on/off ratio equal to 10⁴. We note that these results correlate with those of the square shaped devices with associated gate material. Observe from Fig. 5 and 6 that the change in the gate shape from square to cross leads to smaller current values. Note also that the cross shaped gate offers a uniform current vector profile across terminals when compared to the square shaped device, as can be observed in Fig. 8a) and b).

Fig. 7 and Fig. 8c) present the TCAD simulation results and current density vector profile for the depletion type junctionless device with the HfO₂ gate material, respectively.

Considering the results in Fig. 7, we observe a sharp decrease in the current values for the same simulation run profiles. After a negative electric potential is applied to get the threshold voltages, a sharp amplitude for the threshold voltage (-0.57V for HfO₂, -4.8V for SiO₂) and a high on/off ratio (10⁸ for HfO₂, 10⁷ for SiO₂) are observed.

We compared three different device structures with two different types in various symmetric and non-symmetric operating conditions. Results show good correlations between the symmetric simulations and the devices behave as a four-terminal switch under the given operating conditions.

We note that the current, voltage, and charge data from these TCAD simulations are used for modeling of the four-terminal device as described in the following two sections.

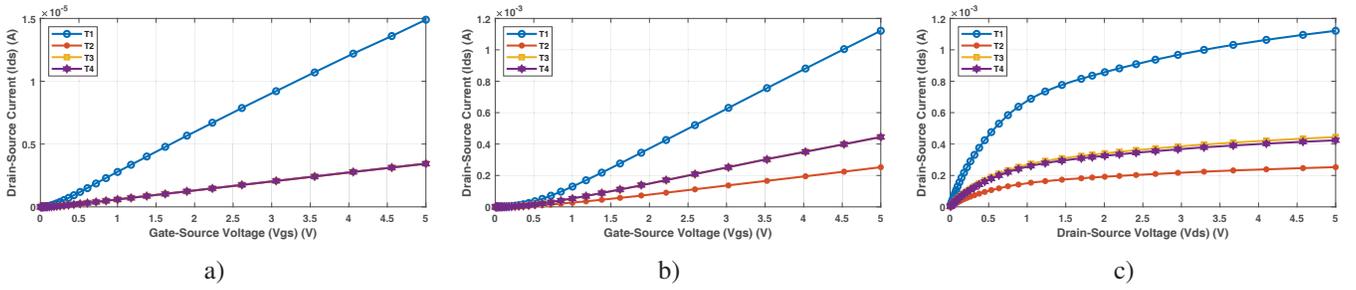


Fig. 5. Results on square shaped device using DSSS case and HfO₂ gate material: a) I_{DS} - V_{GS} with $V_{DS} = 10\text{mV}$; b) I_{DS} - V_{GS} with $V_{DS} = 5\text{V}$; c) I_{DS} - V_{DS} with $V_{GS} = 5\text{V}$.

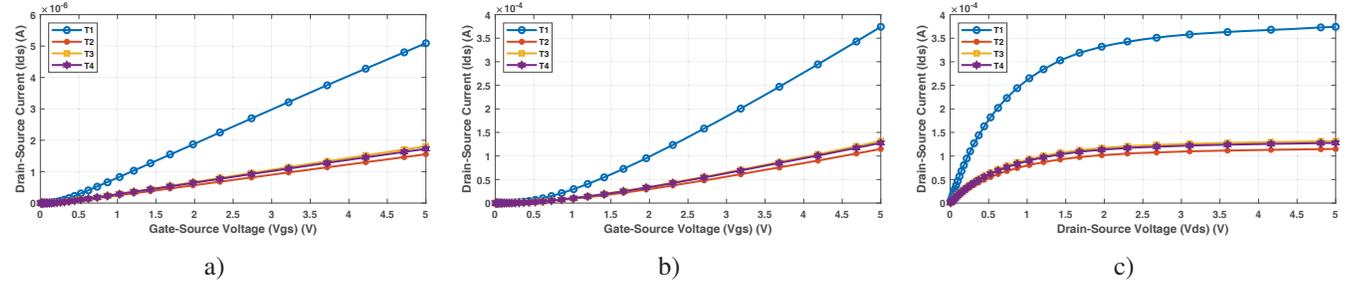


Fig. 6. Results on cross shaped device using DSSS case and HfO₂ gate material: a) I_{DS} - V_{GS} with $V_{DS} = 10\text{mV}$; b) I_{DS} - V_{GS} with $V_{DS} = 5\text{V}$; c) I_{DS} - V_{DS} with $V_{GS} = 5\text{V}$.

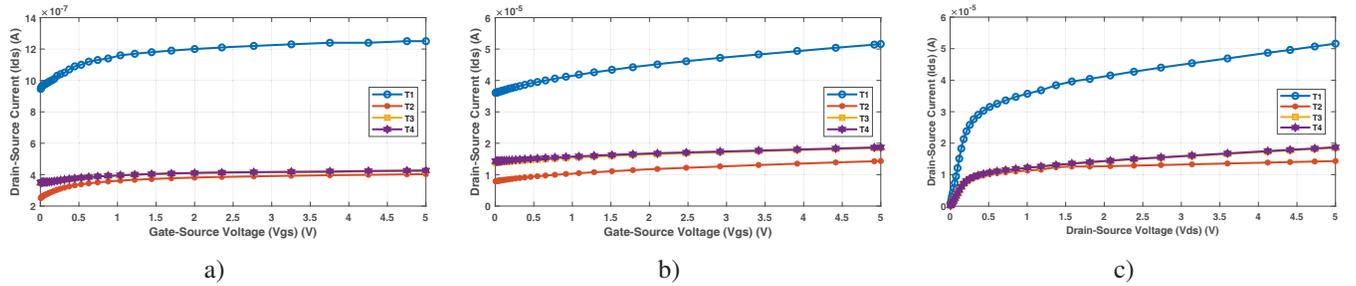


Fig. 7. Results on junctionless device using DSSS case and HfO₂ gate material: a) I_{DS} - V_{GS} with $V_{DS} = 10\text{mV}$; b) I_{DS} - V_{GS} with $V_{DS} = 5\text{V}$; c) I_{DS} - V_{DS} with $V_{GS} = 5\text{V}$.

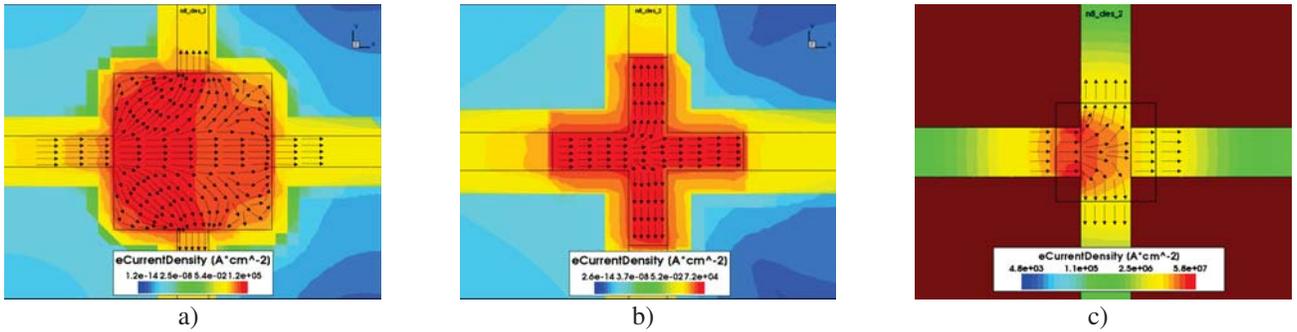


Fig. 8. Current density vector profiles under electric field on different devices: a) square shaped; b) cross shaped; c) junctionless.

IV. MODELING OF SWITCHING LATTICES

In this work, we focus on the modeling of the square shaped device due to its high current value with respect to other devices, considering it as a challenging task. We fit the TCAD simulation data to the MOSFET equations and extract the MOSFET parameters which are used in the circuit level SPICE simulation as described in the next section.

According to the TCAD simulations and the material properties, the basic MOSFET model of the device is designed as a SPICE model circuit which consists of n-type MOSFETs

as shown in Fig. 9. Note that this model is generic and can be applied to the cross shaped and junctionless devices easily. In this model, the level-1 MOSFET equations are given as follows:

$$I_{DS} = \begin{cases} 0 & V_{GS} \leq V_{th} \\ K_p \frac{W}{L} [(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}](1 + \lambda V_{DS}) & V_{GS} > V_{th}, V_{DS} \leq V_{GS} - V_{th} \\ \frac{1}{2} K_p \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) & V_{GS} > V_{th}, V_{DS} > V_{GS} - V_{th} \end{cases}$$

where $K_p = \mu_n C_{ox}$ and μ_n stands for the mobility, C_{ox} denotes the capacitance of the oxide layer, L and W is the

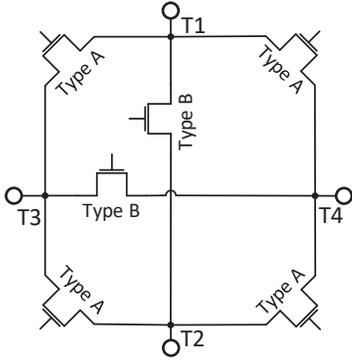


Fig. 9. Model for the square shaped four-terminal switch.

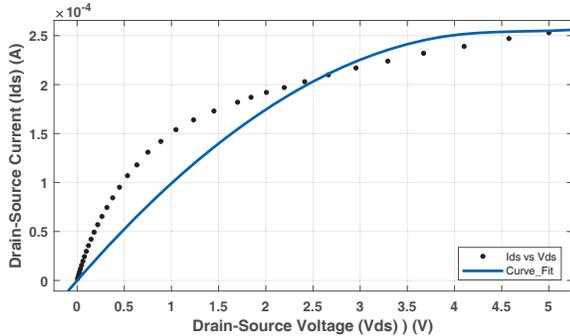


Fig. 10. I-V characteristic of the square shaped four-terminal switch based on the TCAD simulation data and the curve fitted accordingly.

channel length and width, respectively, and λ is the channel length modulation.

In the design of a four-terminal switch, one of the main objectives is to ensure that the I-V characteristic in between any two terminals is the same. We observed from the TCAD simulations that this objective is not satisfied in the square shaped device, due to its geometry. Hence, we decided to use two different MOSFET types, called as Type A and Type B as shown in Fig. 9. Note that these MOSFET types are different from each other according to their effective L values. In the MOSFET model of the square shaped device, L is $0.35\mu\text{m}$ and $0.5\mu\text{m}$ in the Type A and Type B MOSFETs, respectively.

Two scenarios were applied to obtain the TCAD simulation data in the DSSS case. In the first scenario, we applied 5V to the terminal one (T1) and 0V to the other 3 terminals, while V_{GS} is swept from 0 to 5V. In the second scenario, while V_{DS} is swept from 0 to 5V on T1, we applied 0V to other 3 terminals and 5V to V_{GS} . Then, we used the MATLAB Curve Fitting ToolboxTM to determine the values of K_p , λ , and V_{th} in the MOSFET equations that fits the TCAD simulation data with the smallest root-mean square error possible. Fig. 10 presents the I_{DS} - V_{DS} behavior obtained during the TCAD simulations on the square shaped device with the HfO₂ gate material under the DSSS case as shown in Fig. 5c) and the curve fitted based on the MOSFET equations given above.

V. CIRCUIT DESIGN WITH SWITCHING LATTICES

In this work, we focus on testing of the square shape device with the HfO₂ gate material for the circuit functionality and the current drive capability using the Spice simulator with the model described in Section IV. Since the body (bulk) terminal

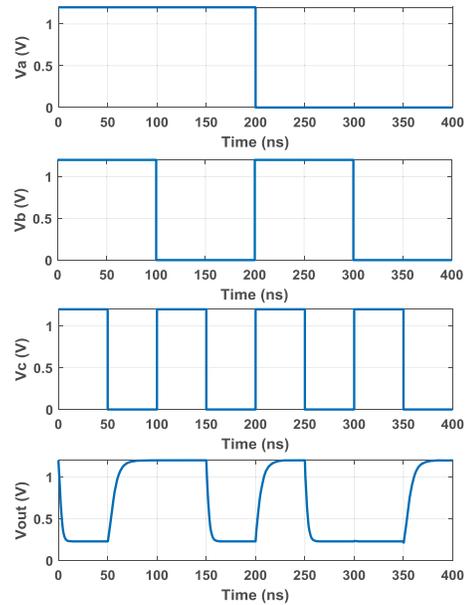


Fig. 11. SPICE transient analysis for the inverse of the XOR₃ gate indicating the circuit functionality.

is always grounded, one of the six terminals is neglected, so the model has five terminals, *i.e.*, four D/S terminal and one gate (control) terminal. We choose to place 1fF grounded capacitor on every terminal that is estimated using the TCAD simulations. The device, also called as circuit, behaves as an n-type switch rather than a p-type switch. Based on the I-V characteristics of the square shape device with the HfO₂ gate material, the supply voltage is set to 1.2V.

We simulate the lattice that realizes the function of XOR₃ gate in Fig. 3b). Considering the lattice size, we place an output capacitor of 10fF. The lattice is simulated by connecting its top plate to a pull-up resistor with a value of 500k Ω . The bottom plate of the lattice is connected to the ground and one end of the resistor is connected to the supply voltage. Note that while the pull-up network is a resistor, the pull-down network is the switching lattice. Thus, the output is negated.

Fig. 11 presents the simulation results. Observe that the lattice operates as expected; it has 0.22V zero-state output voltage. The rise and fall times are approximately 11.3ns and 4.7ns, respectively. These preliminary results are satisfactory but, to make a more concrete statement, simulations should be performed with more accurate transistor model having capacitor models. This is planned as a future work.

As mentioned in Section II, a four-terminal lattice network has a great potential of implementing a logic function with a small number of switches. However, the methodology suggests that the implementation should occur in a whole network rather than using separate gates. This raises a question that how many switches in series the circuit can drive. In order to test this, currents are recorded at constant voltage (1.2V) with an increasing number of switches in series. Results are shown in Fig. 12a). This test is repeated to observe the voltage requirement to have a constant current 5.5 μA . The records are shown in Fig. 12b). These tests give insights on the power consumption, driving current, and circuit complexity.

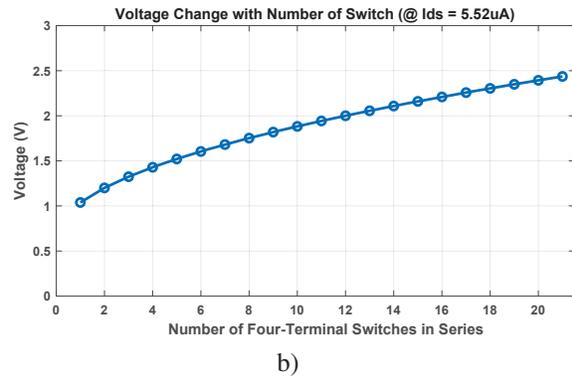
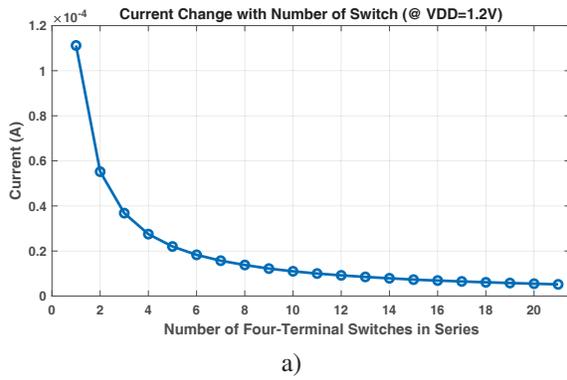


Fig. 12. a) Current flow at constant voltage 1.2V; b) voltage requirement to obtain constant current $5.5\mu\text{A}$ versus number of switches in series.

In a constant voltage test, the current starts at $11.12\mu\text{A}$ and decreases dramatically till $2.2\mu\text{A}$ from 1 to 5 switches. For the number of switches in between 5 and 11, it stays in between $2\mu\text{A}$ and $1\mu\text{A}$. Finally, it reaches $0.52\mu\text{A}$ for 21 switches. We took current constant at $5.5\mu\text{A}$, the value for two switches at 1.2V. In the constant current test, values increase almost linearly till 2.5V for 21 switches. These results clearly indicate that it is feasible to use a considerably large lattice, since the required supply voltage does not change linearly with the number of switches in series.

VI. LESSONS LEARNED AND FUTURE PLANS

In this paper, we study on the simulation and modeling of four-terminal switch based devices with different shapes and gate materials. We then use simulation results in Spice models for circuit-level analysis. As a future work, we plan fabrication studies to validate the simulation results for single devices with different modes. Afterwards, we plan to fabricate a four-terminal switch based nanoarrays.

A. Modeling and Circuit Analysis/Synthesis Plan

We plan to perform more in-depth analysis of four-terminal switch digital circuits using a more accurate model with more specific equations, such as level-3 and BSIM, which includes more precise gate and terminal capacitors and short-channel effect. This analysis should include power consumption, delay (maximum frequency), phase margin, and area. We foresee the capability of using four-terminal lattice for a pull-up network, as used for a pull-down network. This complementary structure obviously makes the static power consumption almost zero and eliminates the dominance of the rise time delay caused by a high pull-up resistor. This means that the circuit can work at high speed with low power consumption and almost zero-voltage logic-zero output state.

Another direction is developing an automated design tool for switching lattices performing performance optimization. With given area, power, delay, and energy specifications, the tool would come up with optimized solutions.

B. Fabrication Plan and Challenges

Fabrication of lithography-based CMOS devices is directly related to the miniaturization steps. Scaling beyond few

nanometers is pushing towards 3D integration and new techniques with area selective atomic layer deposition. The key aspect of designs based on four-terminal devices is the wiring of the gates to perform complex operations. Structure has to be firm and stable in order to apply gate voltage properly. Gate-all-around, monolithic 3D [14], and fine grained vertical 3D [15] like structures may be employed for enabling dense wiring. These are planned for both fabrication and simulation runs for comparison.

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