Wayne P. Burleson

Citizenship: U.S.A.
Birth date: July 3, 1960, Seattle, Washington
Four children (ages 26, 23, 20, 17)

ADDRESSES
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SELECTED RECENT PUBLICATIONS and PATENTS:

Redshift: Manipulating Signal Propagation Delay via Continuous-Wave Lasers
K Yamashita, B Cyr, K Fu, W Burleson, T Sugawara
IACR Transactions on Cryptographic Hardware and Embedded Systems, 2022, 463-489

Programmable access-controlled and generic erasable PUF design and its applications
C Jin, W Burleson, M van Dijk, U Rührmair
Journal of Cryptographic Engineering, 1-20, 2022

Voltage Sensor Implementations for Remote Power Attacks on FPGAs
S Moini, A Deric, X Li, G Provelengios, W Burleson, R Tessier, D Holcomb
ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2021

Cybersecurity of Hospitals: discussing the challenges and working towards mitigating the risks
ST Argaw, JR Troncoso-Pastoriza, D Lacey, MV Florin, F Calcavecchia, et al.
BMC Medical Informatics and Decision Making 20 (1), 1-10 2020.

Grand Challenges for Embedded Security Research in a Connected World
W Burleson, K Fu, D Anthony, J Guajardo, C Gunter, K Ingols, JB Jeannin, et al
arXiv preprint arXiv:2005.06585, 2020

Cost-effective and flexible asynchronous interconnect technology for GALS systems
D Bertozzi, G Miorandi, A Ghiribaldi, W Burleson, G Sadowski
IEEE Micro 41 (1), 69-81. 2021

Reconfiguring the Mux-Based Arbiter PUF using FeFETs
S Ramanujam, W Burleson
2021 22nd International Symposium on Quality Electronic Design (ISQED), 257-262

Dynamic variable precision computation
G Sadowski, W Burleson
US Patent 10,592,207, 2020

EDUCATION

PHD in Electrical Engineering, **University of Colorado**, Boulder, CO. 12/89.
Thesis: Efficient Computation in VLSI with Distributed Arithmetic.
Advisor: Professor Louis L. Scharf

MSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.
Thesis: A Programmable Bit-serial Signal Processing Chip.
Advisors: Professor Campbell L. Searle and Richard F. Lyon (Fairchild).

BSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.
(completed simultaneously with MSEE in 5 years in VI-A co-op program)

EMPLOYMENT

9/05-present **University of Massachusetts Amherst**,
Professor of Electrical and Computer Engineering.

9/23-12/23 **Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland**
Visiting Professor of Electrical Engineering. Research in Hardware Security, Biosensors, SRAM Circuits, and Logic Synthesis. Hosted by G. DeMicheli.

1/13- 6/17 **Advanced Micro Devices, AMD Research, Boxboro, MA**, Senior Fellow in Low-power Design, Led DOE-funded research in supercomputing for 2020 and beyond. This work led to the recent Frontier and El Capitan supercomputers at Oak Ridge and Livermore National Labs. These hold the title for the Greenest and most powerful supercomputer in the world at 2 ExaFLOPs respectively. Led Technology Transfer into AMD product lines. Including work on thermal models, thermal sensing, cooling solutions, on-chip variation modeling and management, on-chip signaling, data-movement energy reduction, GPU compute, efficient pipelining, low-voltage design. Sole PI on a $3M DOE contract on super-computer system integration.

8/12-12/12 **Advanced Micro Devices, AMD Research, Boxboro, MA**, Senior Consultant in Low-power design.

7/11-7/12 **RAMbus, Sunnyvale, CA**. Senior Consultant in Security Engineering.

9/10-5/11 **Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland**
Visiting Professor of Electrical Engineering. Research in 3D VLSI, Biosensors, Hardware Security and RFID Circuits

9/98-3/11 **Intel Corporation, Massachusetts Microprocessor Design Center, (formerly Alpha Development Group of Digital, Compaq, HP)**, Shrewsbury/Hudson, MA.
Consultant on on-chip sensing, soft-errors, clocking, interconnect circuits, low power and design techniques for advanced microprocessors.

9/96-8/05 **University of Massachusetts Amherst**,
Associate Professor of Electrical and Computer Engineering.
Research in the Design and Implementation of Signal Processing and Communication Systems.
Research in Advanced CMOS Circuit Design. Development of Multimedia Courseware,
Educational Co-Director of CASA, an NSF Engineering Research Center.
Teaching of VLSI Design, VLSI Design Project, Embedded Systems Design, Multimedia Systems and Introduction to Programming.

9/03-12/03 **University of Montpellier II, France, Laboratoire des Informatique, Robotique et Microelectronique (LIRMM)**. Montpellier, FRANCE

Visiting researcher on the topics of on-chip interconnect modeling and reconfigurable computing.

7/01-2/05 **National Technological University** (now a division of Laureate Inc. On-line Higher Education), Baltimore, MD.
Curriculum Chair of Computer Engineering, member of Academic Executive Committee.

5/00-8/10 **Datafusion/Tensorcomm Corporations**, Northglenn, CO.
Consultant on cryptography, cellular and GPS implementations in ASIC, FPGA and DSP.

9/96-8/97 **Ecole Nationale Superieure des Telecommunications, Paris, France**.
Sabbatical leave as a visiting professor in the Departmente Electronique.
Research in Adaptive VLSI for Wireless Communications. Innovative teaching involving Internet-based embedded system design project between ENST/Paris, UMASS/Amherst and Pusan National University, South Korea.

9/90-8/96 **University of Massachusetts, Amherst**
Assistant Professor of Electrical and Computer Engineering.
Conducted NSF-funded research in VLSI Timing Design, Array Architectures for DSP/Arithmetic and Computer-Aided Design. Developed new courses in Embedded Systems, VLSI Architecture, VLSI for Digital Signal Processing and VLSI Logic Synthesis. Developed new curricula for VLSI Design sequence, Digital Design and HW Organization. Developed video short courses in VHDL/Verilog and Computer Systems Manufacturing.

1/87-8/90 **University of Colorado,** Boulder, CO.
Research assistant in digital signal processing laboratory. Work involved development of a design methodology for decomposing DSP algorithms at the bit level leading to highly parallel VLSI implementations. Included full-custom design, fabrication and test of a 138,000 transistor CMOS chip. Funding provided by Ball Aerospace and ONR.

8/86-12/86 **University of Colorado,** Boulder, CO.
Teaching assistant in circuits and communications laboratories.

8/83-8/86 **VLSI Technology Inc.**, San Jose, CA.
Architecture, instruction set design and implementation of a CMOS signal processing chip for telecommunications applications. Full-custom design of address generation hardware, internal bus interface and instruction cache and decoder. Architectural specification and design of a CMOS signal processor. Work on this 120,000 transistor chip involved instruction set, logic and circuit design with extensive simulation at all levels. Specific tasks included design of an instruction cache, multi-port register files and a fast hardware implementation of transcendental functions (see Patents).

1/83-5/83 **Massachusetts Institute of Technology**, Cambridge, MA.
Teaching assistant for a course in circuits and network theory.

6/82-1/83 **Fairchild Research and Development**, Palo Alto, CA.
Design and layout of a special purpose signal processing chip in an NMOS technology. Involved design and simulation at the functional, logic and circuit level. Chip was functional on first silicon prototype. (see Master's thesis)

6/81-8/81 **Fairchild Research and Development**, Palo Alto, CA.
Design and simulation of bipolar SRAM cells. Extensive use of SPICE for analog simulation.

RESEARCH SUMMARY

Dr. Burleson has been working in the area of VLSI Design since 1982. His work has included research, development, teaching and industrial work at a variety of levels including theory, algorithms, architectures, systems, circuits and CAD tools. Dr. Burleson is currently Professor of Electrical and Computer Engineering at the University of Massachusetts at Amherst where he has been since 1990. From 2013-2017 he was also Senior Fellow in Low-Power Design for AMD Research, leading DOE-funded research in supercomputing for 2020 and beyond, and leading Technology Transfer into AMD product lines. Since then he has focused on Hardware Security and multi-disciplinary issues in Medical Device Security.

He received his BSEE and MSEE from MIT in 1983 and his PhD from the University of Colorado, 1989. He worked as a custom DSP chip designer for 4 years for VLSI Technology Inc. and Fairchild Semiconductor. He has consulted with Intel, Compaq, HP, Rambus, AMD, and startups Tensorcomm and Datafusion. He was a visiting professor at the Ecole Nationale Superieure des Telecommunications in Paris from September 1996 to August 1997 and with the Laboratoire de Informatique, Robotique et Microelectronique (LIRMM) de Montpellier in Fall of 2003. In 2011 he became Fellow of the IEEE for contributions to integrated circuit design and signal processing, and is a member of ASEE, ACM and Sigma Xi.

Prof. Burleson has conducted VLSI and DSP research funded by NSF, SRC, ARL, Sharp and Intel and has published over 220 journal and conference papers in the following areas: Reconfigurable Communications, VLSI for Communications and Digital Signal Processing; Low-Power Design, Hardware Emulation of Real-Time Systems; Co-design and co-verification of Hardware-Software Systems; Computer Arithmetic, VLSI for Data Compression, Error-Correction, Cryptography, RFID Systems, Scheduling, Path Control, Protocols; Bit-level Algorithms and Mappings to VLSI and FPGA Architectures. Prof. Burleson also leads research in engineering education funded by NSF. He was the education co-director of an NSF Engineering Research Center at UMASS. He leads a multi-disciplinary multi-campus research group in the area of Embedded Security with applications in Transportation, Supply Chain, Medical and Government.

AWARDS

UMass Amherst Chancellor's Medal and Distinguished Lecturer 2022

IEEE Fellow, 2011

College of Engineering Outstanding Junior Faculty Award, 1996

Best Paper Awards at ISVLSI, FIE and other IEEE, ASEE and ACM conferences.

TEACHING

Burleson has taught VLSI design, emphasizing power efficiency and timing analysis, for over 3 decades but has also led development of curriculum in Embedded Systems and Security Engineering. He has developed and currently teaches a required undergraduate lab course in Security Engineering, and graduate courses in Security Engineering, Cryptography and Trustworthy Computing. He also manages the Security certificate at MS level. And in terms of outreach, he has developed curricular materials in Security for High School students and Girl Scout programs.

Courses Taught :
197H Multimedia Systems (a new course for non-majors)
122 Introduction to Programming in C++ (VIP∗)
221 Digital Logic Design (VIP)
232 Hardware Organization and Design (VIP)
371 Introduction to Security Engineering
494 Professional Seminar
551 Computer Systems Lab
558/658 Intro to VLSI / VLSI Design Principles (VIP)
559/659 VLSI Design Project
597M Distributed Application Design in Java
547/647 Security Engineering (On-Line)
556/656 Intro to Cryptography (On-Line)
644 Trustworthy Computing (Remote Live)
664 VLSI Architecture (VIP)
666 Computer Arithmetic (VIP)
697D VLSI Signal Processing
697D Advanced Topics in VLSI (w/ Ciesielski and Koren)
697G Logic Synthesis
697V VLSI Circuit Design
697W Special Topics in Wireless Communications (co-taught with Wireless Communication Center)

(∗ VIP indicates that the course was also offered live through the Video Instructional Program to off-campus students, and in most cases was also available for several additional semesters as a pre-taped distance education course. 558/658 is also available in a novel CD/DVD format developed here at UMASS)

Significant Curriculum Developments

2022 New modules on AI Security, Secure Enclaves, Multi-factor Authenticadtion, Template Attacks, EM Attacks.

2020 New modules on Meltdown/Spectre, Power analysis and Password attacks, and SSD security.

2018 New on-line versions of Security Engineering and Cryptography. 7 week summer/winter versions to allow student flexibility.

2017 New required junior-level course in Security Engineering ECE 371, with lab based on Altera DE1 SOC Board.

2015 New curricular content on Automotive security, voting, cyber-physical systems.

2014 Updates to VLSI Design (ECE 558/658) including new lectures and labs on Networks on Chip, post-CMOS, Hardware Security, and a Case-study on AMD/Microsoft Xbox System on Chip.

2009 New course in Security Engineering (ECE 547/647) building on new UMass research in Embedded Security. 40 students from ECE, CompSci and Civil Engineering. Offered again in 2010, 2012, 2013 (PhD student Georg Becker), 2014 (co-taught with C. Paar).

2005 New course in Embedded Computing Systems (ECE354) incorporating new labs with embedded soft processors, sensor DSP, secure networking and low-power design.

2003 Engineering problems for Introduction to C++ 122

2002 New VLSI special topics course 697V (offered on top of required teaching load)

2001 New course in Multimedia Systems for non-majors. New labs and web/CD-based format.

2001 Web-based course for Professional Seminar 494

2001 Distributed Software Development using Java in 597M

2000 WebDVD Modules for Multimedia Systems 197H, a new course for the minor in Information Technology

1999-present Web-based VLSI Project course integrating recent research 559/659

1999 New multi-disciplinary course in Wireless Communications

1998 MIPS Web tutorial and VHDL Web tutorial in 232

1997 International Design project involving Umass, ENST/Paris and Pusan University, Korea

1995 Video short course in VHDL/Verilog

1995 Video short course in Computer System Manufacturing

1995 Field Programmable Logic from Altera, PIC Microcontrollers, Advanced DSPs from Texas Instruments in 551

1994 New course in VLSI Architecture 664

1992 New course in VLSI Logic Synthesis 697G

1991 New course in VLSI Signal Processing 697D

SERVICE TO THE DEPARTMENT, COLLEGE AND UNIVERSITY

COE Personnel Committee 2021-2022

ECE Committee on On-line Courses 2020-2022

ECE Committee on Joint ECE/CS Curriculum 2021-2022

ECE Graduate Program Committee 2021-2022

ECE DEI committee 2020-2021

ECE Faculty Search Committees on Embedded Systems, Security and Computer Architecture 2021, 2019, 2018, 2013, 2011

ECE Committee on Undergraduate Process and Program (ABET). 03- 13

ECE ECE Faculty Search Committee on Bio-Medical Engineering 2014-15

University Faculty Senate Committee on On-Line Learning and Continuing Education 04-08

Advisory Board Professional Education for Engineering and Applied Science (PEEAS) 02-06

ECE Graduate Curriculum Committee 03-10

ECE Personnel Committee , 90-91, 09-10, 06-07 (chair)

Cadence and Synopsys CAD tool liason 2000-present (coordinate licensing, setup and maintanence of commercial CAD tools used by 8 ECE faculty in research and teaching)

ECE Department Accreditation ABET 2000 Task Force 1999- (one of 5 members guiding the department effort toward meeting and measuring newly revised accreditation criteria)

University Task Force on Information Technology Program 2001- present (Steering Committee and Committees on Curriculum and Capstone Course)

ECE Computer Systems Engineering Senior Design Project Review Board 02-03

Massachusetts Teachers Association Bargaining Team on Distance Learning 2000

University Information Technologies Planning Committee 95-97

University Council on Teaching, Learning and Instructional Technology 94-97

ECE Instructional Development Committee 94-99, 03-present

IEEE Student Branch Advisor 93-95: Developed new seminar series. Developed WWW pages for local branch and IEEE region 1.

College of Engineering, Engineering Computer Services (ECS) Advisory Board 92-96

MOSIS VLSI Fabrication Liaison 91- present

ECE Department Head Search Committee 94

CSE Qualifying Exam Committee 90-04 (responsible twice a year for Algorithms exam),

Massachusetts Microelectronics Center Liaison 91-93

College of Engineering Curriculum Committee 91-92

ECE Graduate and Undergraduate Curriculum Committee 91-92

PROFESSIONAL ACTIVITIES

Fellow of IEEE, "for contributions in integrated circuit design and signal processing". Member of Signal Processing Society. Member of Circuits and Systems Society, Member of Computer Society, Member since 1984, Senior Member since 2001. Fellow since 2011.

Co-organizer and founder of the first New England Security Day, Sept 17, 2015 in Amherst. A one-day workshop on Cybersecurity co-organized with Computer Science, School of Management and Math. Attended by 113 faculty and students from the greater New England area. Organized and chaired a panel on Hardware Security.

Chair of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), involves planning and coordination of SIPS workshops, ICASSP reviews, award nominations. 2004-2006.

Steering Committee, Program Committee and Posters Chair for *IEEE Conference on Microelectronic Systems Education (MSE)*, 2003,2005,2007

Associate Editor, *IEEE Transactions on VLSI*, 1998-2003

Associate Editor, *ACM Transactions on the Design Automation of Electronic Systems*, (an on-line journal), 1998-2001

Member of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), 97-present

Co-Chair, 1998 IEEE VLSI Signal Processing Workshop, Boston. w/ K. Konstantinides.

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 2000. w/ E. Manolakos

Guest Editor Special Issue on Reconfigurable Computing in DSP Systems of *the Journal of Signal Processing Systems*, Summer 2000. w/ N. Shanbhag

Guest Editor Special Issue on VLSI in Wireless Networks in *ACM Wireless Networks*, Spring 1998. w/ M. Steyaert

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 1998. w/ K. Konstantinides.

Editorial Board of *Journal of VLSI Signal Processing Systems*, 1995-.

Editorial Board of IEEE Press Series on Microelectronic Systems, 1997-

Associate Editor *IEEE Transactions on Circuits and Systems, II*., 1994-95.

Technical Program Co-Chair, 1996 IEEE VLSI Signal Processing Workshop, San Francisco w/ K. Konstantinides

Program Committees: ISCAS 95,96; VSP 94,96; SIPS 01, ASAP 94,95,96,97,00,02; TAU 95, ISLPED 97,98

Organizer of a Forum on Wave-pipelining at the 1994 IEEE International Symposium on Circuits and Systems.

Member of Association of Computing Machinery 95-

Member of Sigma Xi 83-

REFEREE/REVIEWER FOR:

National Science Foundation, (panels on CISE CAREER, EIA, ERC and Design Automation)
Swiss National Science Foundation
French National Science Foundation
Austrian National Science Foundation
Korean National Science Foundation

IEEE Transactions on Circuits and Systems,
IEEE Transactions on Signal Processing,
IEEE Transactions on Computers,
IEEE Transactions on VLSI,
Journal of VLSI Signal Processing.
IEEE Signal Processing Magazine,
Computer Magazine,
Intl. Symposium on Circuits and Systems,
Intl. Conference on Computer Design,
Intl. Conference on Computer Aided Design,
Intl. Conference on Acoustics, Speech and Signal Processing,
Intl. Symposium on Low-Power Electronics and Design,
Design Automation Conference,
VLSI Design Conference,
VLSI Signal Processing Workshop (now Workshop on Signal Processing Systems),
Conference on Application-Specific Array Processors,
Great Lakes Symposium on VLSI.
Cryptographic Hardware and Embedded Systems

PUBLICATIONS (for complete list, please refer to Google Scholar or DBLP)

The total number of citations on Googlescholar as of October 2022 was approximately 101,108 with h-index of 47 and of i10-index of 153.

For a complete list, see https://dblp.org/pid/b/WaynePBurleson.html or https://scholar.google.com/citations?hl=en&user=jwCp7QUAAAAJ