GRADUATE STUDENTS with Theses completed under supervision of Wayne Burleson

April 2025

Current PhD Students:

24. Negin Mohajerri. Memristor Circuits for High Performance Edge ML (started January 2025)
23. Mohammed Faheemur Memristor Circuits for Secure and Robust ML (started September 2024)

Current MS Students:

Ph.D. Graduates:

22. Shayan Moini, 2022. FPGA Side-channels (now at Qualcomm), co-advised with R. Tessier
21. Shuo Li: 2019. Time Difference Circuits (now Apple)
20. Xiaolin Xu: 2017. Physical Unclonable Functions (now Assistant Professor, Northeastern U.)
19. Raghavan Kumar: 2015. Physical Unclonable Functions (now at Intel Circuits Research Lab)
18. Gesine Hinterwalder: 2015. Lightweight Elliptic Curve Implementations (co-advised w/ C. Paar)
17. Vikram Suresh: 2015. True Random Number Generation (was at Intel, Circuits Research Lab)
16. Georg Becker: 2014. Intentional and Unintentional Side-Channels in Embedded Systems (co-advised by C. Paar) (now in Germany)
15. Lang Lin 2012: Cryptography in Nanometer CMOS (now at Ansys)
14. Basab Datta, 2010: Thermal Effects and On-Chip Sensors (now at Netronome)
13. Jinwook Jang, 2011: Jitter in On-Chip Interconnects (now at Cavium)
12. Vishak Venkatraman 2008, Multi-level Current Signaling, (now at Apple)
11. Matt Heath: 2006. Synchro-tokens, (returned to position at Intel)
10. Atul Maheshwari. 2004: Current-mode Circuits for Long Interconnects , (Intel Advanced Technology)
9. Lt. Col. Andrew Laffely 2004: Configurable Computing for Low-Power Signal Processing, now faculty at US Air Force Academy, Colorado Springs.
8. Jeongseon Euh 2002: 3D Graphics acceleration (Samsung Semiconductor, Portable Products Group)
7. Andres Garcia Garcia. 1999, Power estimation in FPGAs, Dean of Engineering at Universite de Tecnologia, Monterey, Mexico (PhD from ENST, Paris)
6. Hyunhee Choi, 1997. Wordlength Optimization, took position as Senior VLSI Designer at Advanced Micro Devices
5. Bongjin Jung, 1996. Array Architectures for Lempel-Ziv Compression, took position as Senior Engineer at Intel
4. Zheng Zhou, 1996. Formal Verification of Datapaths, took position as CAD Researcher at Silicon Graphics Inc.
3. Taek-Soo Kim, 1995 Wave-pipelining, Techniques and Tools, now Manager at Samsung Semiconductor
2. Mircea Stan, 1995. Low-Power Interconnects took position at University of Virginia, now Professor and IEEE Fellow
1. Yongjin Jeong, 1994. Array Algorithms and Architectures for Finite Field Arithmetic, took position at Samsung, now Professor at Kwangwoon University, South Korea

M.Sc. thesis Graduates:

43. Max Cohen Hoffing, FPGA Power Transient measurement
42.Yuhe Zhao, Return Pointer Authentication in RISC-V
41. Zhe Xu, Block Chain for Pharmaceutical Supply Chain (continuing in UMass PhD)
40. Matt Burke, Power Delivery Network PUFs (MITRE)
39. Jackie Lagasse: Power Side-channel Countermeasures (MITRE)
38. Shweta Malik: Layout-level Hardware Obfuscation Tool (Intel)
37. Mark Buckler: Synchronization Issues in Network on Chip (PhD program at Cornell, startup)
36. Vinay Patel: 3D Power Supply Modeling (PhD program at UMass)
35. Mehrenosh Dabiowala: PVT Impacts on Wearout (Intel)

34. Vikram Suresh: True Random Number Generation (continued PhD w/ Burleson, Intel)
33. Sudheendra Srivaths: Physically Unclonable Functions in Nanometer CMOS (IBM)
32. Ashwin Lakshminarsinham: EM Side-Channel Analysis for Watermarking (Intel)
31. Krishna Chillara: Signal Techniques for Through-Silicon Vias (now at Intel)
30. Mike Todd: Hardware Emulation of Secure RFID Sensors (now at Intel, AZ))
29. Serge Zhilyaev: Applied Cryptography for RFID (took position at Intel, AZ)
28. Xiang Yun: Thermal Sensor Placement (continued to PhD at U. Michigan)
27. Lang Lin: Leakage-based Power Analysis (continued in PhD program with Burleson, now at Ansys)
26. Venkatesh Arunachalam (Clock Distribution in 3D Microprocessor), (took position at SUN Microsystems/Oracle)
25. Ibis Benito: Global Interconnects in the Presence of Uncertainty, (started UMass PhD, now at Intel)
24. Dan Holcomb: SRAM for Chip ID and TRNG (Berkeley Phd, now faculty at UMass)
23. Basab Datta: Thermal Sensors (continuing in UMASS PhD program)
22. Sheng Xu: Current-sensed interconnects (took position at Analog Devices, then MBA, now at BASF)
21. Jinwook Jang (Jitter in On-Chip Interconnects) (continuing in UMass PhD program)
20. Chris Cowell: Interconnect-driven Architectural Performance optimization (took position at Intel)
19. Aiyappan Natarajan: Content-addressable Memory for Smart Cards (took position at AMD)
18. Jeevan Chittamuru: Content-adaptive Texture-mapping for 3Dgraphics (took position at .Qualcomm)
17. Vijay Shankar: Leakage and Variations in On-Chip Caches (took position at Qualcomm, then MBA, now at Tile)
16. Srividya Srinivasaraghavan: Interconnect Effort (took position at Intel)
15. Sriram Srinivasan: Current-mode Circuits for Long Interconnects (took position at AMD)
14. Manoj Sinha: Current-mode Circuits for RAMs (took position at Micron)
13. Santosh Thampuram: CD/DVD-based Distance Learning Technology (took position at Bloomburg)
12. Atul Maheshwari: Current-mode Circuits for Long Interconnects: (took position UMASS PhD, now at Intel)
11. Prashant Jain: Content-Aware Low-power VLSI Video Coding (took position UMASS PhD)
10. Subramanian Venkatraman: Power-Aware DSP Architectures and Tools (took position at Intel)
9. Chandrika Duggirala: Tools to Support Flexible Modular Curricula (took position at Motorola)
8. Anki Nalamalpu , Repeater Design in DSM CMOS (took position at Intel, Hillsboro, MA)
7. Nitin Srimal, Indexing of Hand-written text and Video. (took position in PhD program at U. Michigan.)
6. Jason Ko, Scheduling Co-processor (VLSI Designer, Hewlett Packard, CA, Transwitch, Neuro…, acquired by Intel?)
5. Bongjin Jung, Array Estimation and Simulation CAD Tools (took position at Intel)
4. Sashi Obilisetty, (founder and CEO of DualSoft, Nashua, NH, since acquired by TransEDA, now Director at Synopsys)
3. Yamini Polisetty, Signal Flow Graph Transformation Tools (took position as CAD Developer, Quantum, MA)
2. Wei-han Lien, Wave-Domino Logic (took position as VLSI Designer, HAL Computer, Sunnyvale, CA, then Apple, now TensTorrent)
1. Walter Marvin, CAD for Optical Computing (took position as OS software consultant, CT)

Recent BS Honor's Thesis Students:

8. Brayden Bergeron, Side-channels Hybrid Attacks, (General Dynamics)
7. Jordan Andrade, Side-channels Template Attacks,
6. Nathan Costa, Side-channels, (Electric Boat and UMass MS on-line)
5. Joe Maloyan, Side-channels, (U Mass MS program)
4. Andrew Hartnett, Fault injections on Ring Oscillators (UMass MS program)
3. Byran Tam, Drone Communication Security (NEU MS program)
2. Matt Caswell, ML Architectures (Apple)
1. Ethan Miller, Fault-injection countermeasures (Raytheon)