Wayne P. Burleson

Citizenship: U.S.A.
Birth date: July 3, 1960, Seattle, Washington
Four children (ages 23, 20, 17, 14)

ADDRESSES

Office:
Knowles Engineering Building, 309B
Department of Electrical and Computer Engineering
University of Massachusetts
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RECENT PUBLICATIONS:

Cybersecurity of Hospitals: discussing the challenges and working towards mitigating the risks
ST Argaw, JR Troncoso-Pastoriza, D Lacey, MV Florin, F Calcavecchia, ...
BMC Medical Informatics and Decision Making 20 (1), 1-10

Grand Challenges for Embedded Security Research in a Connected World
W Burleson, K Fu, D Anthony, J Guajardo, C Gunter, K Ingols, JB Jeannin, ...
arXiv preprint arXiv:2005.06585

Guest Editorial Special Section on Security Challenges and Solutions With Emerging Computing Technologies
A Chattopadhyay, S Ghosh, W Burleson, D Mukhopadhyay
IEEE Transactions on Very Large Scale Integration (VLSI) Systems 27 (11 …

When the Physical Disorder of CMOS Meets Machine Learning
X Xu, S Li, R Kumar, W Burleson
Low Power Semiconductor Devices and Processes for Emerging Applications in …

Dynamic variable precision computation
G Sadowski, W Burleson
US Patent 10,592,207

EDUCATION

PHD in Electrical Engineering, **University of Colorado**, Boulder, CO. 12/89.
Thesis: Efficient Computation in VLSI with Distributed Arithmetic.
Advisor: Professor Louis L. Scharf

MSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.
Thesis: A Programmable Bit-serial Signal Processing Chip.
Advisors: Professor Campbell L. Searle and Richard F. Lyon (Fairchild).

BSEE **Massachusetts Institute of Technology**, Cambridge, MA. 6/83.

(completed simultaneously with MSEE in 5 years in VI-A co-op program)

EMPLOYMENT

9/05-present **University of Massachusetts Amherst**,
Professor of Electrical and Computer Engineering.

1/13- 6/17 **Advanced Micro Devices, AMD Research, Boxboro, MA**, Senior Fellow in Low-power Design, Led DOE-funded research in supercomputing for 2020 and beyond. This work led to the recent El Capitan supercomputer at Livermore, Los Alamos, Sandia, the most powerful supercomputer in the world at 2 ExaFLOPs. Led Technology Transfer into AMD product lines. Including work on thermal models, thermal sensing, cooling solutions, on-chip variation modeling and management, on-chip signaling, data-movement energy reduction, GPU compute, efficient pipelining, low-voltage design. Sole PI on a $3M DOE contract on super-computer system integration.

8/12-12/12 **Advanced Micro Devices, AMD Research, Boxboro, MA**, Senior Consultant in Low-power design.

7/11-7/12 **RAMbus, Sunnyvale, CA**. Senior Consultant in Security Engineering.

9/10-5/11 **Ecole Polytechnique Federale de Lausanne (EPFL), Switzerland**
Visiting Professor of Electrical Engineering. Research in 3D VLSI, Biosensors, Hardware Security and RFID Circuits

9/98-3/11 **Intel Corporation, Massachusetts Microprocessor Design Center, (formerly Alpha Development Group of Digital, Compaq, HP)**, Shrewsbury/Hudson, MA.
Consultant on on-chip sensing, soft-errors, clocking, interconnect circuits, low power and design techniques for advanced microprocessors.

9/96-8/05 **University of Massachusetts Amherst**,
Associate Professor of Electrical and Computer Engineering.
Research in the Design and Implementation of Signal Processing and Communication Systems.
Research in Advanced CMOS Circuit Design. Development of Multimedia Courseware,
Educational Co-Director of CASA, an NSF Engineering Research Center.
Teaching of VLSI Design, VLSI Design Project, Embedded Systems Design, Multimedia Systems and Introduction to Programming.

9/03-12/03 **University of Montpellier II, France, Laboratoire des Informatique, Robotique et Microelectronique (LIRMM)**. Montpellier, FRANCE
Visiting researcher on the topics of on-chip interconnect modeling and reconfigurable computing.

7/01-2/05 **National Technological University** (now a division of Laureate Inc. On-line Higher Education), Baltimore, MD.
Curriculum Chair of Computer Engineering, member of Academic Executive Committee.

5/00-8/10 **Datafusion/Tensorcomm Corporations**, Northglenn, CO.
Consultant on cryptography, cellular and GPS implementations in ASIC, FPGA and DSP.

9/96-8/97 **Ecole Nationale Superieure des Telecommunications, Paris, France**.
Sabbatical leave as a visiting professor in the Departmente Electronique.
Research in Adaptive VLSI for Wireless Communications. Innovative teaching involving Internet-based embedded system design project between ENST/Paris, UMASS/Amherst and Pusan National University, South Korea.

9/90-8/96 **University of Massachusetts, Amherst**
Assistant Professor of Electrical and Computer Engineering.
Conducted NSF-funded research in VLSI Timing Design, Array Architectures for DSP/Arithmetic and Computer-Aided Design. Developed new courses in Embedded Systems, VLSI Architecture, VLSI for Digital Signal Processing and VLSI Logic Synthesis. Developed new curricula for VLSI Design sequence, Digital Design and HW Organization. Developed video short courses in VHDL/Verilog and Computer Systems Manufacturing.

1/87-8/90 **University of Colorado,** Boulder, CO.
Research assistant in digital signal processing laboratory. Work involved development of a design methodology for decomposing DSP algorithms at the bit level leading to highly parallel VLSI implementations. Included full-custom design, fabrication and test of a 138,000 transistor CMOS chip. Funding provided by Ball Aerospace and ONR.

8/86-12/86 **University of Colorado,** Boulder, CO.
Teaching assistant in circuits and communications laboratories.

8/83-8/86 **VLSI Technology Inc.**, San Jose, CA.
Architecture, instruction set design and implementation of a CMOS signal processing chip for telecommunications applications. Full-custom design of address generation hardware, internal bus interface and instruction cache and decoder. Architectural specification and design of a CMOS signal processor. Work on this 120,000 transistor chip involved instruction set, logic and circuit design with extensive simulation at all levels. Specific tasks included design of an instruction cache, multi-port register files and a fast hardware implementation of transcendental functions (see Patents).

1/83-5/83 **Massachusetts Institute of Technology**, Cambridge, MA.
Teaching assistant for a course in circuits and network theory.

6/82-1/83 **Fairchild Research and Development**, Palo Alto, CA.
Design and layout of a special purpose signal processing chip in an NMOS technology. Involved design and simulation at the functional, logic and circuit level. Chip was functional on first silicon prototype. (see Master's thesis)

6/81-8/81 **Fairchild Research and Development**, Palo Alto, CA.
Design and simulation of bipolar SRAM cells. Extensive use of SPICE for analog simulation.

RESEARCH SUMMARY

Dr. Burleson has been working in the area of VLSI Design since 1982. His work has included research, development, teaching and industrial work at a variety of levels including theory, algorithms, architectures, systems, circuits and CAD tools. Dr. Burleson is currently Professor of Electrical and Computer Engineering at the University of Massachusetts at Amherst where he has been since 1990. From 2013-2017 he was also Senior Fellow in Low-Power Design for AMD Research, leading DOE-funded research in supercomputing for 2020 and beyond, and leading Technology Transfer into AMD product lines.

He received his BSEE and MSEE from MIT in 1983 and his PhD from the University of Colorado, 1989. He worked as a custom DSP chip designer for 4 years for VLSI Technology Inc. and Fairchild Semiconductor. He has consulted with Intel, Compaq, HP, Rambus, AMD, Tensorcomm and Datafusion. He was a visiting professor at the Ecole Nationale Superieure des Telecommunications in Paris from September 1996 to August 1997 and with the Laboratoire de Informatique, Robotique et Microelectronique (LIRMM) de Montpellier in Fall of 2003. In 2011

he became Fellow of the IEEE for contributions to integrated circuit design and signal processing, and is a member of ASEE, ACM and Sigma Xi.

Prof. Burleson has conducted VLSI and DSP research funded by NSF, SRC, Sharp and Intel and has published over 200 journal and conference papers in the following areas: Reconfigurable Communications, VLSI for Communications and Digital Signal Processing; Low-Power Design, Hardware Emulation of Real-Time Systems; Co-design and co-verification of Hardware-Software Systems; Computer Arithmetic, VLSI for Data Compression, Error-Correction, Cryptography, RFID Systems, Scheduling, Path Control, Protocols; Bit-level Algorithms and Mappings to VLSI and FPGA Architectures. Prof. Burleson also leads research in engineering education funded by NSF. He was the education co-director of an NSF Engineering Research Center at UMASS. He led a multi-disciplinary multi-campus research group in the area of Embedded Security with applications in Transportation, Supply Chain, Medical and Government.

TEACHING

Burleson has taught VLSI design, emphasizing power efficiency and timing analysis, for over 3 decades but has also led development of curriculum in Embedded Systems and Security Engineering. He has developed and currently teaches a required undergraduate lab course in Security Engineering, and graduate courses in Security Engineering, Cryptography and Trustworthy Computing. He also manages the Security certificate at MS level. And in terms of outreach, he has developed curricular materials in Security for High School students and Girls Scout programs.

Courses Taught :
197H Multimedia Systems (a new course for non-majors)
122 Introduction to Programming in C++ (VIP∗)
221 Digital Logic Design (VIP)
232 Hardware Organization and Design (VIP)
494 Professional Seminar
551 Computer Systems Lab
558/658 Intro to VLSI / VLSI Design Principles (VIP)
559/659 VLSI Design Project
597M Distributed Application Design in Java
664 VLSI Architecture (VIP)
666 Computer Arithmetic (VIP)
697AB Security Engineering
697D VLSI Signal Processing
697D Advanced Topics in VLSI (w/ Ciesielski and Koren)
697G Logic Synthesis
697V VLSI Circuit Design
697W Special Topics in Wireless Communications (co-taught with Wireless Communication Center)

(∗ VIP indicates that the course was also offered live through the Video Instructional Program to off-campus students, and in most cases was also available for several additional semesters as a pre-taped distance education course. 558/658 is also available in a novel CD/DVD format developed here at UMASS)

Significant Curriculum Developments

2020 New modules on Meltdown/Spectre, Power analysis and Password attacks, and SSD security.

2018 New on-line versions of Security Engineering and Cryptography. 7 week summer/winter versions to allow student flexibility.

2015 New curricular content on Automotive security, voting, cyber-physical systems.

2014 Updates to VLSI Design (ECE 558/658) including new lectures and labs on Networks on Chip, post-CMOS, Hardware Security, and a Case-study on AMD/Microsoft Xbox System on Chip.

2009 New course in Security Engineering (ECE 697AB) building on new UMass research in Embedded Security. 40 students from ECE, CompSci and Civil Engineering. Offered again in 2010, 2012, 2013 (PhD student Georg Becker), 2014 (co-taught with C. Paar).

2005 New course in Embedded Computing Systems (ECE354) incorporating new labs with embedded soft processors, sensor DSP, secure networking and low-power design.

2003 Engineering problems for Introduction to C++ 122

2002 New VLSI special topics course 697V (offered on top of required teaching load)

2001 New course in Multimedia Systems for non-majors. New labs and web/CD-based format.

2001 Web-based course for Professional Seminar 494

2001 Distributed Software Development using Java in 597M

2000 WebDVD Modules for Multimedia Systems 197H, a new course for the minor in Information Technology

1999-present Web-based VLSI Project course integrating recent research 559/659

1999 New multi-disciplinary course in Wireless Communications

1998 MIPS Web tutorial and VHDL Web tutorial in 232

1997 International Design project involving Umass, ENST/Paris and Pusan University, Korea

1995 Video short course in VHDL/Verilog

1995 Video short course in Computer System Manufacturing

1995 Field Programmable Logic from Altera, PIC Microcontrollers, Advanced DSPs from Texas Instruments in 551

1994 New course in VLSI Architecture 664

1992 New course in VLSI Logic Synthesis 697G

1991 New course in VLSI Signal Processing 697D

SERVICE TO THE DEPARTMENT, COLLEGE AND UNIVERSITY

ECE Faculty Search Committee on Bio-Medical Engineering 2014-15

ECE Faculty Search Committees on Embedded Systems, Security and Computer Architecture 2013, 2011

ECE Committee on Undergraduate Process and Program. 03- present

University Faculty Senate Committee on On-Line Learning and Continuing Education 04-08

Advisory Board Professional Education for Engineering and Applied Science (PEEAS) 02-06

ECE Graduate Curriculum Committee 03-present

ECE Personnel Committee , 09-10, 06-07 (chair), 90-91

Cadence and Synopsys CAD tool liason 2000-present (coordinate licensing, setup and maintanence of commercial CAD tools used by 8 ECE faculty in research and teaching)

ECE Department Accreditation ABET 2000 Task Force 1999- (one of 5 members guiding the department effort toward meeting and measuring newly revised accreditation criteria)

University Task Force on Information Technology Program 2001- present (Steering Committee and Committees on Curriculum and Capstone Course)

ECE Computer Systems Engineering Senior Design Project Review Board 02-03

Massachusetts Teachers Association Bargaining Team on Distance Learning

University Information Technologies Planning Committee 95-97

University Council on Teaching, Learning and Instructional Technology 94-97

ECE Instructional Development Committee 94-99, 03-present

IEEE Student Branch Advisor 93-95: Developed new seminar series. Developed WWW pages for local branch and IEEE region 1.

College of Engineering, Engineering Computer Services (ECS) Advisory Board 92-96

MOSIS VLSI Fabrication Liaison 91- present

ECE Department Head Search Committee 94

CSE Qualifying Exam Committee 90-04 (responsible twice a year for Algorithms exam),

Massachusetts Microelectronics Center Liaison 91-93

College of Engineering Curriculum Committee 91-92

ECE Graduate and Undergraduate Curriculum Committee 91-92

PROFESSIONAL ACTIVITIES

Fellow of IEEE, "for contributions in integrated circuit design and signal processing". Member of Signal Processing Society. Member of Circuits and Systems Society, Member of Computer Society, Member since 1984, Senior Member since 2001. Fellow since 2011

Co-organizer of the first New England Security Day, Sept 17, 2015 in Amherst. A one-day workshop on Cybersecurity co-organized with Computer Science, School of Management and Math. Attended by 113 faculty and students from the greater New England area. Organized and chaired a panel on Hardware Security.

Chair of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), involves planning and coordination of SIPS workshops, ICASSP reviews, award nominations. 2004-2006.

Steering Committee, Program Committee and Posters Chair for *IEEE Conference on Microelectronic Systems Education (MSE)*, 2003,2005,2007

Associate Editor, *IEEE Transactions on VLSI*, 1998-2003

Associate Editor, *ACM Transactions on the Design Automation of Electronic Systems*, (an on-line journal), 1998-2001

Member of IEEE Signal Processing Society Technical Committee on the Design and Implementation of DSP Systems (DISPS), 97-present

Co-Chair, 1998 IEEE VLSI Signal Processing Workshop, Boston. w/ K. Konstantinides.

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 2000. w/ E. Manolakos

Guest Editor Special Issue on Reconfigurable Computing in DSP Systems of *the Journal of Signal Processing Systems*, Summer 2000. w/ N. Shanbhag

Guest Editor Special Issue on VLSI in Wireless Networks in *ACM Wireless Networks*, Spring 1998. w/ M. Steyaert

Guest Editor Special Issue on Recent Advances in the Design and Implementation of DSP Systems of *the Journal of Signal Processing Systems*, Winter 1998. w/ K. Konstantinides.

Editorial Board of *Journal of VLSI Signal Processing Systems*, 1995-.

Editorial Board of IEEE Press Series on Microelectronic Systems, 1997-

Associate Editor *IEEE Transactions on Circuits and Systems, II.*, 1994-95.

Technical Program Co-Chair, 1996 IEEE VLSI Signal Processing Workshop, San Francisco w/ K. Konstantinides

Program Committees: ISCAS 95,96; VSP 94,96; SIPS 01, ASAP 94,95,96,97,00,02; TAU 95, ISLPED 97,98

Organizer of a Forum on Wave-pipelining at the 1994 IEEE International Symposium on Circuits and Systems.

Member of Association of Computing Machinery 95-

Member of Sigma Xi 83-

INVITED TALKS (not updated since 2014)

Cybersecurity Risk Analysis: A Multi-disciplinary Challenge, ACSC Cybersecurity Risk Analysis Workshop at MIT, Cambridge, MA, September 2014

Colloquium Speaker, Brown University, Computer Science, "RFID Privacy: From Transportation Payments to Implantable Medical Devices", April 2014

Keynote, Workshop on Embedded Systems Security (WESS), "RFID Privacy: From Transportation Payments to Implantable Medical Devices", Montreal, September 2013,

Colloquium Speaker, Dartmouth College Computer Science, "RFID Privacy: From Transportation Payments to Implantable Medical Devices", September, 2013

Keynote, RFID Security and Privacy Workshop, Graz, Austria, "RFID Privacy: From Transportation Payments to Implantable Medical Devices", **July 2013**

Tutorial, DATE 2013, Grenoble. "Systems Issues in E-Health Devices", March 2013

Keynote of SOC-SIC Colloquium, Lyon, France, "Hardware Security in Nanometer CMOS", June 2011.

IMEC, Belgium "On-Chip Sensors: An Enabling Technology for Multi-core and 3D integration", April 2011.

Keynote, Workshop on CMOS Variability, Grenoble, France "On-Chip Sensors: An Enabling Technology for Multi-core and 3D integration", May 2011.

IEEE Medical and Communication Technology, Montreux, Switzerland, "Physical Security with Ultra Wideband". March 2011. **(Invited Talk)**

ETHZ, Zurich, Switzerland, "Lightweight Security and Privacy for Implantable Medical Devices", April 2011.

ENST, Paris, France, "Hardware Security in Nanometer CMOS", April 2011

LIRM, Montpelier, France, "Hardware Security in Nanometer CMOS", February 2011

Ecole des Mines, Gardanne, France, "Hardware Security in Nanometer CMOS", February 2011

EPFL EE Summer School, "Hardware Security in Nanometer CMOS", June 2011

University Jean Monnet, St. Etienne, France, "Hardware Security in Nanometer CMOS", December 2010.

ETHZ, Zurich, Switzerland. "Hardware Security in Nanometer CMOS", December 2010.

CSEM, Neuchatel, Switzerland, "Hardware Security in Nanometer CMOS", November 2010.

Ruhr University, Bochum, Germany, "Hardware Security in Nanometer CMOS", October 2010.

KU Leuven, Belgium , "Hardware Security in Nanometer CMOS", October 2010.

EPFL, Lausanne, Switzerland, "Hardware Security in Nanometer CMOS", October 2010.

Eurecom/ENST, Sophia Antipolis, France, "RFID Innovations at the Bottom", June 2009.

EPFL, Lausanne, Switzerland, "Thermal Sensing and Management", May 2009.

Intel Fault Aware Computing Group, "On-Chip Sensors: A Survey", March 2009.

Intel Circuits Research Lab, Hillsboro, OR, "CMOS Computation in the Presence of Uncertainty: Modelling, Measuring, and Mitigating Variations", September, 2008

Intel Fault Aware Computing Group, "NBTI Wearout: Models, Measurements and Mitigation", March 2008.

EPFL, Lausanne, Switzerland, "Statistical Interconnect Design", June 2006.

ENST/Nice, France, "RFID Security and Privacy: A Hardware Perspective", June 2006

U. of Patras, Patras Greece, "Circuits and Architectures for On-Chip Interconnects",May 2005.

Intel, Hudson, MA "Parity Prediction Circuits", April 2005.

Keynote Address at Boston Area Architecture Conference, Brown University, " Performance, Energy and Reliability Tradeoffs in Deep Sub-Micron CMOS VLSI", January 2005.

Chalmers University, Sweden, "Circuits for Long On-Chip Interconnects", December 2003.

LIRMM, University of Montepellier, France, "Synchrotokens", December, 2003.

ENST, Paris, France, "Adaptive System on a Chip for Low-Power Signal Processing", December, 2003.

LIRMM, University of Montepellier, France, "Circuits for Long On-Chip Interconnects", January 2003.

University of Bretagne Sud, L'Orient France, "Adaptive System on a Chip for Low-Power Signal Processing. May 2001 (part 2 in May 2002)

INSA Toulouse, France, "Current-Mode Circuits for Long Interconnect". May 2001.

LIRMM, University of Montepellier, France, "Current-Mode Circuits for Long Interconnect". May 2001. (part 2 in May 2002)

Intel, Circuits Research Lab, Hillsboro, Oregon, August 2001, "Current-Mode Circuits for Long Interconnects".

Smith College, October 1999, " Educational Innovations in Multimedia Systems".
A similar presentation also made at the Asynchronous Learning Networks Conference in College Park, Maryland, November 1999 and to the UMass College of Engineering Dean's Advisory Council, November 1999.

Alpha Development Group, Compaq Computer Corporation, June 1999, " RLC Circuits for VLSI Designers" (a 6 hour short course).

Alpha Development Group, Compaq Computer Corporation, April 1999, "A Case for Current-Mode in Long Interconnects".

Intel, Circuits Research Lab, Hillsboro, Oregon, June, 1998, "Circuits for Long Interconnects".

ENST, Paris, FRANCE, May, 1998, "Reconfiguration for Power Savings in Real-time Motion Estimation".

IRISA, Rennes, FRANCE, February, 1997, "Reconfigurable Communications Systems".

Motorola Research Center, Paris, FRANCE, April, 1997, "Reconfigurable Communications Systems".

IMEC, Leuven, BELGIUM, May 1997, "Reconfigurable Communications Systems".

Lecture tour in SOUTH KOREA, including Samsung Semiconductor, ETRI National Lab, Korean Advanced Institute of Science and Technology (KAIST), Pusan National University. "Advanced VLSI in Communications Systems", June, 1996. Funded by NSF, ETRI and Samsung.

Digital Semiconductor, Hudson, MA, “Low-Power CMOS VLSI Techniques", November, 1995

University of Utah, “VLSI Signal Processing: Systems Designs and CAD Tools", March 1995

Stanford University, “Wave-pipelining: A New Objective in High-Performance VLSI Design?", April 1994.

NEC, C.C. Research Labs, Princeton, New Jersey, “VLSI Signal Processing Research at UMass/Amherst", December 1994.

University of Colorado, “Coordinating VLSI Design, CAD Development and Communications Systems Design", October 1994.

Queens University, Belfast, Northern Ireland, “Using Regular Array Methods for DSP Module Synthesis", June 1994.

Ecole Nationale Superieure des Telecommunication (ENST), Paris, France. “Using Regular Array Methods for DSP Module Synthesis", May 1994.

Northeastern University, “ARREST: A Graphical Design Environment for VLSI Arrays", April 1993

University of Utah, “VLSI Research at UMass/Amherst", March 1992

Tufts University, “Structured VLSI Synthesis", February 1992

University of Colorado, “Structured VLSI Synthesis for DSP", October 1991

REFEREE/REVIEWER FOR:

National Science Foundation, (panels on CISE CAREER, EIA and Design Automation)
Swiss National Science Foundation
French National Science Foundation
Austrian National Science Foundation
Korean National Science Foundation

IEEE Transactions on Circuits and Systems,
IEEE Transactions on Signal Processing,
IEEE Transactions on Computers,
IEEE Transactions on VLSI,
Journal of VLSI Signal Processing.
IEEE Signal Processing Magazine,
Computer Magazine,
Intl. Symposium on Circuits and Systems,
Intl. Conference on Computer Design,
Intl. Conference on Computer Aided Design,
Intl. Conference on Acoustics, Speech and Signal Processing,
Intl. Symposium on Low-Power Electronics and Design,
Design Automation Conference,
VLSI Design Conference,
VLSI Signal Processing Workshop (now Workshop on Signal Processing Systems),
Conference on Application-Specific Array Processors,
Great Lakes Symposium on VLSI.
Cryptographic Hardware and Embedded Systems

PUBLICATIONS (for complete list, please refer to Google Scholar or DBLP)

Below is a partial list of Books, Book Chapters, Refereed Conference papers and Journal papers. The total number of citations on Googlescholar as of February 2021 was approximately 10,500 with h-index of 45 and of i10-index of 156.

For a complete list, see https://dblp.org/pid/b/WaynePBurleson.html or https://scholar.google.com/citations?hl=en&user=jwCp7QUAAAAJ

BOOKS:

B1) *VLSI Signal Processing X*, T. Meng, K. Konstantinides, W. Burleson, IEEE Press. 1996. A collection of 40 leading papers on the design and implementation of signal processing systems.

B2) *Signal Processing Systems*, E. Manolakos, A. Chandrakasan, L.G. Chen, K. Konstantinides, W. Burleson, IEEE Press, 1998. A collection of 40 leading papers on the design and implementation of signal processing systems.

B3) *Security and Privacy in Implantable Medical Devices*, W. Burleson and S. Carrara, Springer, 2014 A collection of 8 papers with contributions from both Bio-Medical Engineering and Security Engineering. Topics include Threat Models, Wireless Security, Bio-Sensors, Safety vs Security Trade-offs.

BOOK CHAPTERS:

BC1) R. Tessier and W. Burleson, "Reconfigurable Computing for Digital Signal Processing" in *Programmble Digital Signal Processors*, Marcel-Dekker (editor, Yu Hen Hu). 2001.

BC2) Mircea R. Stan, Wayne P. Burleson, "Bus-Invert Coding for Low-Power I/O", pp. 296-305, in *Low-power CMOS Design* edited by Anantha Chandrakasan, Robert Brodersen, IEEE Press, 1998.

BC3) Raghavan Kumar, Xiaolin Xu, Wayne Burleson, Sami Rosenblatt, and Toshiaki Kirihata; Physically Unclonable Functions: A Window into CMOS Process Variations; Circuits and Systems for Security and Privacy. Jun 2016 , 183 -244

JOURNALS:

Published or to appear:

J1) W. Burleson, L. Scharf, N. Endsley and A. Gabriel, "A Systolic VLSI Chip for Implementing Orthogonal Transforms", *Journal of Solid State Circuits*, Vol.24, No. 2, (April, 1989), pp. 466-468.

J2) W. Burleson, "Polynomial Evaluation in VLSI with Distributed Arithmetic", *IEEE Transactions on Circuits and Systems*, October, 1990, pp. 1299-1302.

J3) W. Burleson and L. Scharf, "A VLSI Design Methodology for Distributed Arithmetic", *Journal of VLSI Signal Processing*, 2 (1991), pp. 235-252.

J4) M. Stan, W. Burleson, C. Connolly, R. Grupen, "Analog VLSI for Robot Path Planning", *Journal of VLSI Signal Processing*, 8, 61-73 (1994).

J5) Y. Jeong, W. Burleson,"VLSI Array Synthesis for Polynomial GCD computation and Application to Finite Field Division", *IEEE Transaction on Circuits and Systems II*, December 1994, Vol 41,

J6) W.-H. Lien, W. Burleson,"Wave-Domino Logic: Theory and Application", *IEEE Transactions on Circuit and Systems II*, February, 1995, Vo. 42, No 2, pp 78-91.

J7) M. Stan, W. Burleson, "Bus-Invert Method for Low-Power I/O",
IEEE Transactions on VLSI Systems, March, 1995, Vo. 3, No 1, pp 49-58.

J8) Y. Jeong and W. Burleson, "Array Algorithms and Architectures for RSA Modular Multiplication based on Precalculated Complements of the Modulus," *IEEE Transactions on VLSI Systems*, June 1997.

J9) M. Stan, W. Burleson "Low-Power Encodings for Global Communication in CMOS VLSI", *IEEE Transactions on VLSI Systems*, vol 5, no 4, Dec. 1997, pp. 444-455.

J10) B. Jung, W. Burleson, "VLSI Algorithm, Architecture and Implementation for High-Speed Lempel-Ziv Data Compression", *IEEE Transactions on VLSI Systems*, Sept 1998.

J11) B. Jung, W. Burleson, "Performance Optimization of Wireless Local Area Networks through VLSI Data Compression", *ACM Wireless Networks* Special Issue on VLSI in Wireless Networks, Winter 1998.

J12) W. Burleson, M. Ciesielski, F. Klass, W. Liu, "Wave-pipelining in VLSI: A Survey and Tutorial", *IEEE Transactions on VLSI Systems*, Sept, 1998.

J13) B. Jung, W. Burleson, "VLSI Architectures for Pyramid Vector Quantization", *Journal of VLSI Signal Processing Systems*, Winter 1998.

J14) W. Burleson, J. Ko, D. Niehaus, K. Ramamritham, J. Stankovic, G. Wallace, C. Weems "The Spring Scheduling Co-Processor: A Scheduling Accelerator" , *IEEE Transactions on VLSI*, November, 1998.

J15) R. Tessier and W. Burleson, "Reconfigurable Computing for Digital Signal Processing: A Survey", *Journal of VLSI Signal Processing Systems*, Fall 2000.

J16) W. Burleson, A. Ganz and I. Harris, "Educational Innovations in Multimedia Systems", *Journal of Engineering Education*, Winter 2000.

J17) A. Nalamalpu, S. Srinivasan, W. Burleson, "Boosters for Global Interconnect: Circuits, Design Methods and Comparison with Repeaters", *IEEE Transactions on Computer Aided Design*, Dec. 2001

J18) A. Maheshwari, W. Burleson and R. Tessier, "Trading-off Transient Fault-tolerance and Power Consumption in Deep Submicron (DSM) VLSI Circuits"**,** *IEEE Transactions on VLSI Systems*, volume 12, Issue 3, pp.299-311, March 2004.

J19) P. Jain,A. Laffely,W. Burleson,R. Tessier,and D. Goeckel,"Dynamically Parameterized Algorithms and Architectures to Exploit Signal Variations", *Journal of VLSI Signal Processing Systems*, vol 36, no. 1, pages 27-40, January 2004.

J21) A. Maheshwari, W. Burleson, "Differential Current Sensing for On-Chip Interconnects", *IEEE Transactions on VLSI Systems.* Volume 12, Issue 12, pp. 1321 – 1329, December 2004.

J20) J. Chittamuru, J. Euh and W. Burleson, "Power-Aware 3D Graphics Rendering", *Journal of VLSI Signal Processing Systems,* January, 2005.

J22) L. Bossuet, G. Gogniat, W. Burleson, "Dynamically Configurable Security for SRAM FPGA Bitstreams", *International Journal of Embedded Systems*. Issue 5/6 of 2005 .

J23) S. Swaminathan, R. Tessier, D. Goeckel, **W. Burleson**, "A Reconfigurable Viterbi Decoder in FPGAs", *IEEE Transactions on VLSI Systems.* Volume 13, Issue 4, pp.484 – 488, April 2005.

J24) M. Heath, **W. Burleson**, I. Harris, "Synchrotokens: A Deterministic GALS Methodology for Chip-Level Debug and Test", *IEEE Transactions on Computers*. Vol. 54, no. 12, December 2005.

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