NIRT: Self-Aligned and Self-Limited Quantum Dot Nanoswitches

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Overview

This NSF NIRT project addresses the fabrication of quantum scale devices. The project aims to demonstrate the validity of nanoscale computing by developing a process technology to fashion quantum dots (QD) of a predictable size, shape and placement, suitable for mass production and simple electrical contacts.

The research spans issues of materials science, circuits, and device fabrication and characterization; the structures to be fabricated are closely integrated with quantum level devices necessary for cellular automata circuits. Methods of high speed testing to characterize the devices as well as theoretical modeling to optimally design the structures are included.

The project is highly collaborative between Ohio State, Illinois, Notre Dame, California at Riverside, and the Naval Research Laboratory. The project addresses basic research issues in a topical area of materials science with high technological relevance. An important feature of the program is the integration of research and education through the training of students in a fundamentally and technologically significant area. The project brings together electrical engineers, material scientists, physicists, computer scientists, experimentalists, and theoreticians for the purpose of realizing advanced nanostructured quantum dot devices.

The project is designed to develop strong technical, communication, and organizational/management skills in students through unique educational experiences made possible by a forefront research environment. There is an active involvement of undergraduates in the program. Cross-disciplinary research and site visits to each other will enhance the educational process.

Project Goals

This project will develop a process technology to fashion QDs of a predictable size, shape and placement, suitable for mass production and which can be readily contacted by external circuitry. Furthermore, our proposed approach greatly relaxes the lithographic tolerances needed to achieve ≤ 10 nm diameter QDs for room temperature switching. The formation of QDs having many of these properties has implications beyond the nanoelectronics community, having impact in medicine, composites, environmental monitoring etc. The interdisciplinary nature of the work involving electrical engineering, materials science, physics and computer science makes this an excellent educational topic for the training of future scientists.

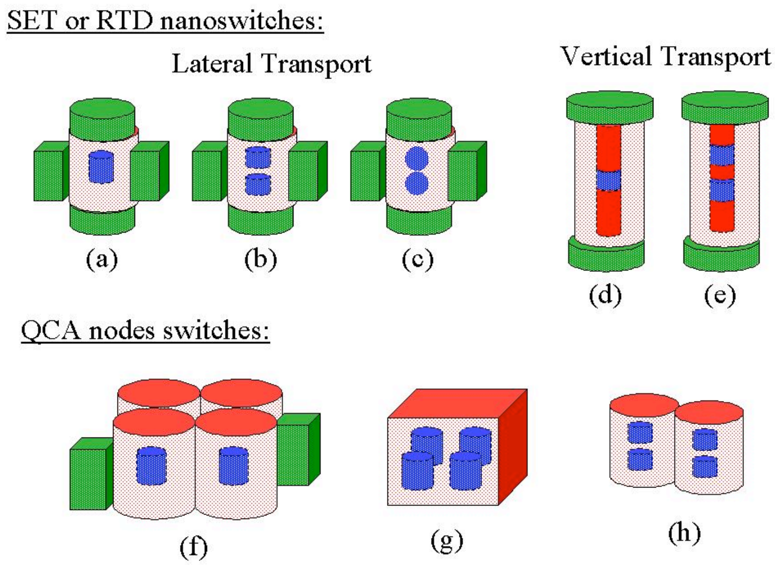

Figure 1. Schematic diagram of the nano-pillars (red cylinders) with embedded quantum dots (small blue cylinders) The light red signifies silicon dioxide and the solid dark red denotes silicon. The external contacts, both lateral and vertical, are illustrated by green disks or blocks.

Potential Applications

This proposed novel process for the formation of QD based switching elements is an enabling technology which can be applied to a variety of circuit architectures, including (i) single-electron tunneling (SET) transistors [1], (ii) resonant tunneling diode (RTD) based circuitry [2], (iii) quantum-dot cellular automata (QCA) [3], and quantum computing [4] . Low-power memory can be explored using an SET configuration while logic may be more appropriate using an RTD or QCA configuration. Our approach to the formation of the QD makes it an attractive approach that is also compatible with existing CMOS technology. Since many RTD-based circuits require driving transistors, this is an important advantage.

An SET can be built using the quantum dot embedded within the nano-pillar as the storage node. A metallic etch mask can be utilized as a self-aligned gate electrode. Contacts beside the nano-pillar can be added for lateral transport (Fig. 1a-c), or vertical transport (Fig. 1d-e) through the pillar can be utilized too by adding a bottom contact. RTDs are essentially large multi-electron SETs, which allow tunneling into and out of the zero-dimensional QD [5].

Nano-pillars can also be assembled into 4-leaf clover clusters, forming QCA nodes (Fig. 1f). For lateral tunneling, metal contacts can then deposited along these sidewalls. Alternative QCA nodes would use multiple QDs inside one larger pillar (Fig. 1g). The most unique approach is a vertical QCA node (Fig. 1h) whereby two QDs are contained within one pillar. The advantages here are that the electron never needs to tunnel out of the pillar and that the vertical stacking permits an even greater packing density. Any background charge can be controlled by external electrodes added adjacent to the pillars.

Recent Results

We have developed an electron beam lithography process from writing nano-scale patterns on a Si/SiGe substrate, a plasma etching recipe, an oxidation process and a transmission electron microscope evaluation process to characterize embedded quantum dots such as that shown below. Concurrently, theoretical modeling of the quantum devices and electrical measurement techniques of the completed devices are being developed.

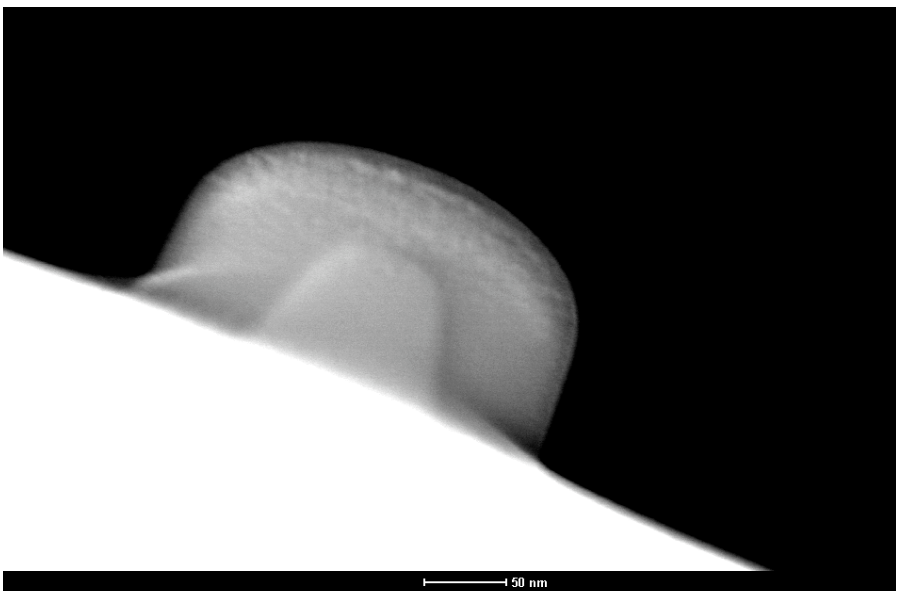

Figure 2. Scanning electron micrograph revealing the QD embedded within a dielectric layer.

References

[1] For further information about this project email pberger@ieee.org.

[2] T. A. Fulton and G. J. Dolan, "Observation of Single-Electron Charging Effects in Small Tunnel Junctions," *Phys. Rev. Lett.*, **59**, pp. 109-112 (1987).

[3] A. Seabaugh, X. Deng, T. Blake, B. Brar, T. Broekaert, R. Lake, F. Morris, and G. Frazier, "Transistors and Tunnel Diodes For Analog/Mixed-Signal Circuits and Embedded Memory," *IEDM Tech. Digest,* **98**, 429 (1998).

[4] P. Douglas Tougaw, Craig S. Lent, Wolfgang Porod, "Bistable saturation in coupled quantum-dot cells", *J. Appl. Phys.*, **74**, pp. 3558-3565, (1993).

[5] Bennett CH, DiVincenzo DP, Smolin JA, Wootters WK, "Mixed-state entanglement and quantum error correction," *Physical Review A*, **54**, pp. 3824-3851 (1996).

[6] T. Fijisawa and S. Tarucha, "Resonant Tunneling Properties of Single Electron Transistors with a Novel Double-Gate Geometery," *Appl. Phys. Lett.*, **68**, pp. 526-529 (1996).